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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Schloesser, et al. Docket No.: INF-135  
Serial No.: 10/777,128 Art Unit: 2818  
Filed: February 13, 2004 Examiner: TBD  
For: Method of Fabricating and Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

**Certificate of Mailing via First Class Mail (37 C.F.R. § 1.8(a))**

Date of Deposit: August 11, 2004

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IDS Form PTO/SB/08a (1 page) citing (7) references  
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Respectfully submitted,

*Natalie Swider*

Natalie Swider  
Legal Assistant

Slater & Matsil, L.L.P.  
17950 Preston Rd., Suite 1000  
Dallas, TX 75252  
Tel: 972-732-1001  
Fax: 972-732-9218



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Mail Stop: Amendment  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Dear Sir:

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08a that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Respectfully submitted,

Ira S. Matsil  
Attorney for Applicants  
Reg. No. 35,272

August 11, 2004

Date

Slater & Matsil, L.L.P.  
17950 Preston Rd., Suite 1000  
Dallas, TX 75252  
(972) 732-1001 (phone)  
(972) 732-9218 (fax)



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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.